MUX-BASED DESIGN OF DPLL FOR WIRELESS COMMUNICATION

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ABSTRACT: - In the modern day communication devices, the main aspect lies in the proper reception of data at minimum possible error rates and also on the highest degrees of precision. But while performing so, a very important aspect that should be kept in mind is the capability of the device developed to operate at reasonable speeds, because it must be compatible with the other sub-systems of the required communication setup. Also, the design complexity of the device as well as the cost of design should be minimum. By putting all these factors together, we can say that the complexity is the main concern of this proposed work. Considering the various problems right now, this paper is done to demonstrate the multiplexer-based DPLL device which comprises of features such as good speed, simplified design and precise reception of data and also some ways to overcome the limitations has been discussed with full interest.

KEYWORDS: - multiplexer, oscillator, detector, phase, recovery, DPLL.

INTRODUCTION: - [1] PLL is an electronic circuit consists of a loop filter, variable frequency oscillator and a phase detector. [2] PLL circuit compares the phase of the input signal with the phase of the frequency of its oscillator to keep the phases matched. The signal from the phase detector is used for controlling the oscillator in a feedback loop. Frequency is also known as the derivative of phase. [3] As a result, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. The former property is used for demodulation, and the latter property is used for indirect frequency synthesis as we know. [4] A DPLL is a digital version of PLL circuit. It has many advantages over the analog PLL specifically with parameters like noise performance and processing. DPLL consists of JK flip flops, a digital phase-frequency detector realized using XOR gates etc. Also, it consists of a Digital Loop Filter which is designed using the basic design procedures for Digital Filters. Also, DPLL has a feedback element which is a discrete time version of a Voltage Controlled Oscillator (VCO) also sometimes known as Digital Controlled Oscillator (DCO) or Numerically Controlled Oscillator (NCO). [5] This feedback element is used to generate the input reference signal. The loop filter is used in the process of removing the high frequency randomness. [6] The DPLL corrects and locks the phase of the incoming signal and the reference signal and due to it the frequencies are also locked giving a replica of the original message pulse at the output with much improved in noise performance and less design complexity.

THEORETICAL BACKGROUND: - The DPLL is a modern-day communication device that performs the role of a receiver in the digital communication setup. DPLL accepts at its input, the signal that comes to the receiver which is corrupted by the noise. The principle DPLL works on is phase matching as it tries to lock the phase of the corrupted incoming pulse by retrieving the received pulse from the corruption caused by the external environment. The block diagram of DPLL is as shown below

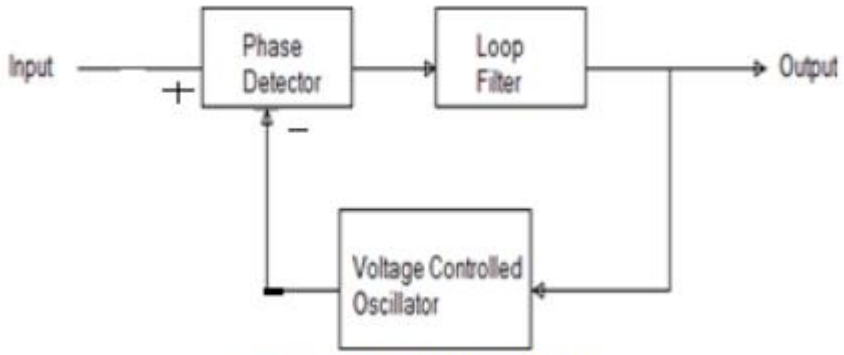

Figure 1: Block Diagram of DPLL

The phase detector detects the phase difference between the incoming signal $X_1(t)$ and the reference signal $X_{ref}(t)$.

$$X_1(t) = A_1 \cos(2\pi f_c t + \theta_i(t)) \quad (1)$$
$$X_{ref}(t) = A_{ref} \cos(2\pi f_c t + \theta_{ref}(t)) \quad (2)$$

where, A_1, A_{ref} are the amplitudes of the incoming signal and reference signal respectively. f_c is the carrier frequency. The output of the phase detector is the multiplication of the incoming signal and the reference signal that is the signal given by equation (1) is multiplied with the signal given by equation (2) and the output of the phase detector is

$$X_m(t) = (A_i A_{ref} \frac{K_d}{2})[\sin\left(2\omega_c t + \theta_i(t) + \theta_{ref}(t)\right) - \sin(\theta_i(t) - \theta_{ref}(t))] \quad (3)$$

where K_d is the multiplier constant.
The output of the phase detector given by equation (3) when passed through the loop filter, the carrier frequency components will be eliminated and hence the output of the phase detector is given by

$$X_{pd}(t) = -\sin(\theta_i(t) - \theta_{ref}(t)) \quad (4)$$

So it is seen that the output of the phase detector given by equation (4) is the phase difference between the incoming signal and the reference signal. When the phases of both the signals are same the output of the phase detector is given by:

$$\lim_{\theta_i \to 0} sin\ \theta_i = 0 \quad (5)$$

The mathematical equation of VCO is given by:-

$$f_{tuning}(t) = K_0 V_{in}(t)$$

Where K_0 is the oscillator gain, V_{in} is the time domain symbol of the control voltage of the VCO.

The block diagram of MUX based DPLL is shown below

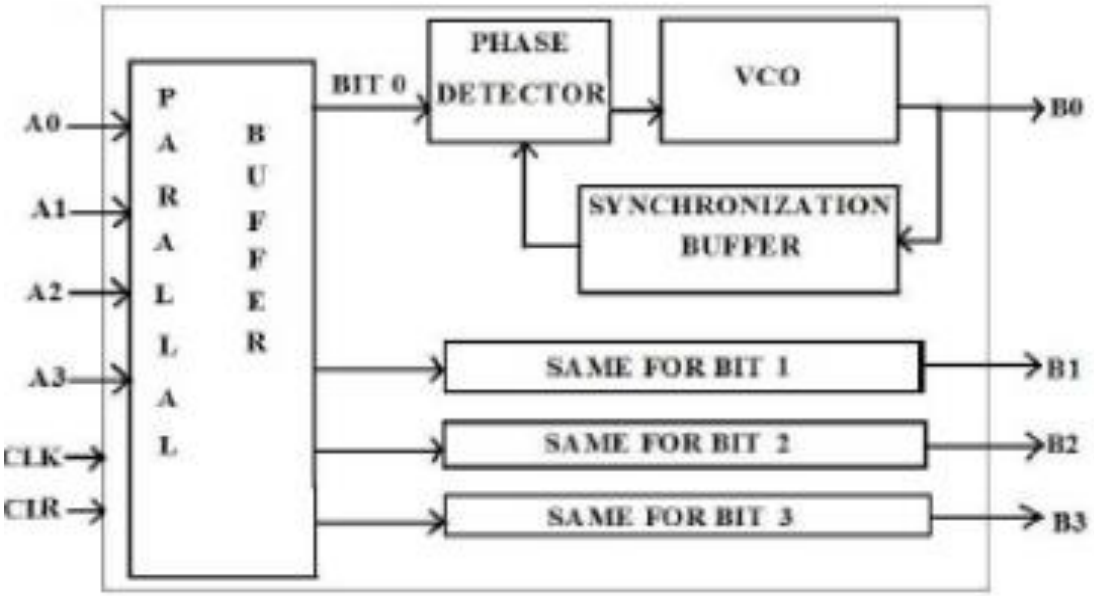

Figure2: Block Diagram of MUX Based DPLL

The purpose of parallel buffer in MUX based DPLL is to feed the data bits to the DPLL within a single clock pulse, the phase detector, which is used to detect the phase in between the input and reference signal. The VCO is to examine whether the phases of the input signal match the reference signal. If it, doesn't it correct the phase and at each clock it locks the incoming signal with that of the reference, for the purpose of synchronization between the input and the reference signals the synchronization buffer is being used. In wireless communication link, the DPLL receiver receives input in analog form. Hence analog to digital conversion (ADC) is used and the ADC output is finally fed to the DPLL receiver input.

WORKING MODEL OF MUX BASED DPLL: - The circuit diagram is shown below

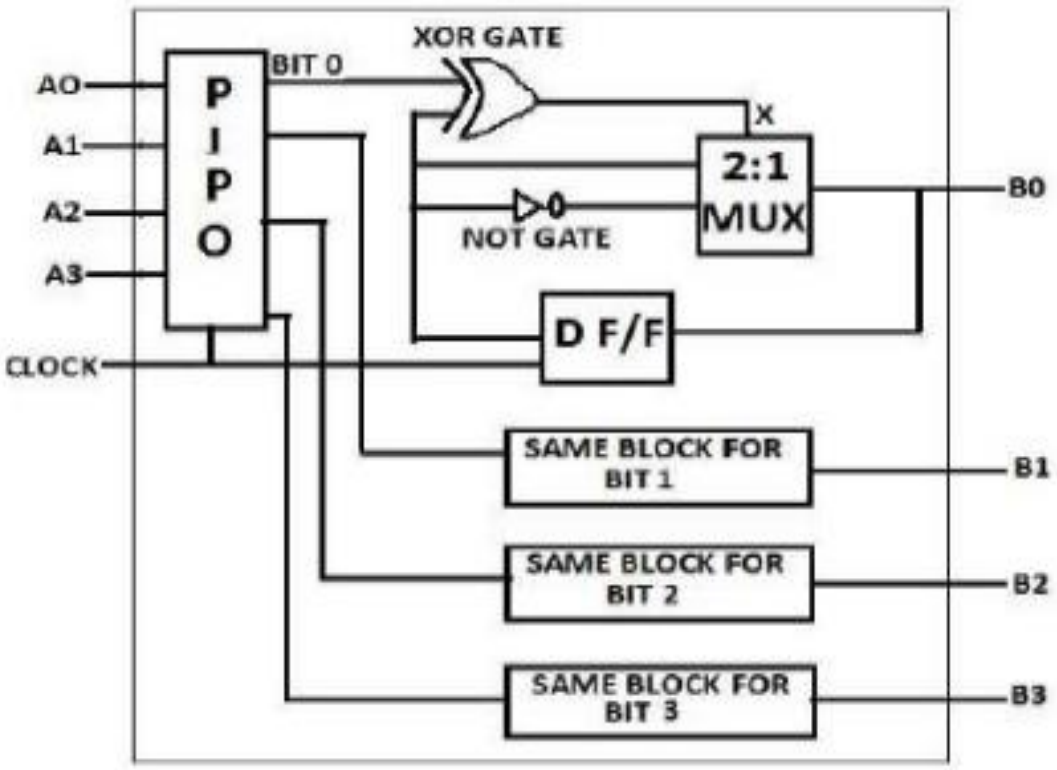

Figure 3: MUX Based DPLL

The explanation is given below:-

- The first block is PIPO and one clock input is fed to DPLL.
- It is followed when the phase detector which has a mismatch between the reference bit and the incoming bit from V_{CO} and will yield '1' or '0'.
- For V_{CO}, 2:1 multiplexer is used to generate the same bit of the input bit. Initially the output of MUX is '0', so if the input bit is '1', then there will be mismatch which will give x=1. So, then output '1' is obtained, because it will select the 2^{nd} input line.
- D FF is used for synchronization

RESULTS AND DISCUSSIONS: - The schematic diagram of the MUX-based DPLL is shown below

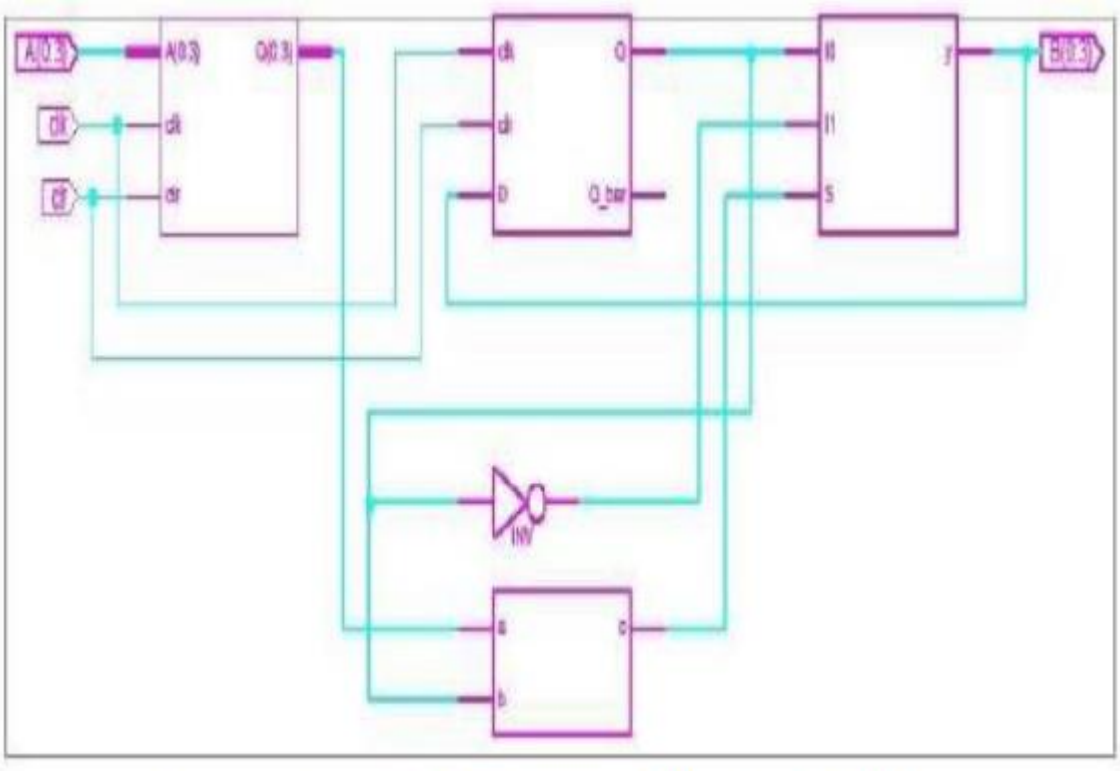

Figure 4: Schematic diagram of MUX-based DPLL

Figure shown above represents the RTL schematic diagram. The four-bit vector represents the corrupted received pulse. The stated 4 bits are processed by PIPO which is used to synchronization for processing. The block is made up of Exclusive OR based phase detectors which finds out whether the reference data bits and input bits are in phase or not. V_{CO} generates reference bits which in turn designed by multiplexer. The bits which are used as reference is feedback to the D flip flop. At the output clock pulse is obtained.

The expected output waveform is as shown below

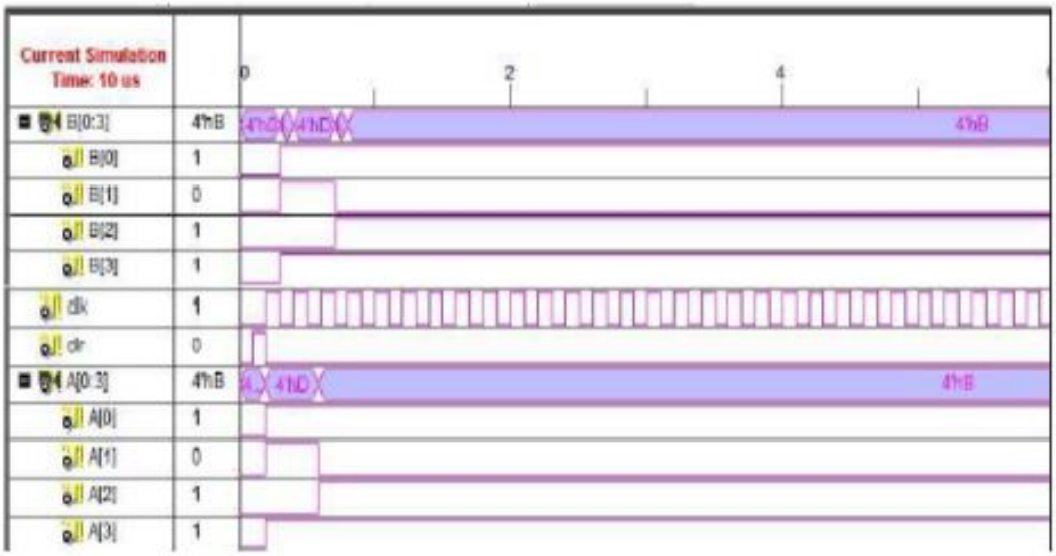

Figure 5: Output Waveform of MUX-Based DPLL

The above figure shows us the timing graph for the mux-based DPLL system, the above figure shows a four bit vector i.e., A (0,3) of input corrupted data. Each part of the vector is plotted as individual waveforms against time. B (0,3) represents the recovered data. This device operates on a single master clock also known as 'clk'. The DPLL recovers the data during the time duration of the clock pulse. For the above design parallel circuitry is used.

ADVANTAGES: -

- The system produces high speed locking. It can operate at high speeds without any speed enhancement circuitry. The main reason is DPLL performs locking action is the single clock pulse duration irrespective of the bit size hence no delay
- The operating principle is very simple and the design is easy, since the circuit consists of fundamental parts thus reducing the cost.

LIMITATIONS: - The demerit of this DPLL is that if the number of bits are very large, the design cost and complexity of the machine increases. This is because parallel circuitry is used for each bit and thus design part increases and thus becomes a problem

METHOD OF OVERCOMING THE SAID LIMITATION: -

The way of overcoming the above limitation is by using counter based DPLL circuit which reduces the complexity of the system by correcting only one bit at a time.

COUNTER BASED DPLL: - The circuit diagram is shown below

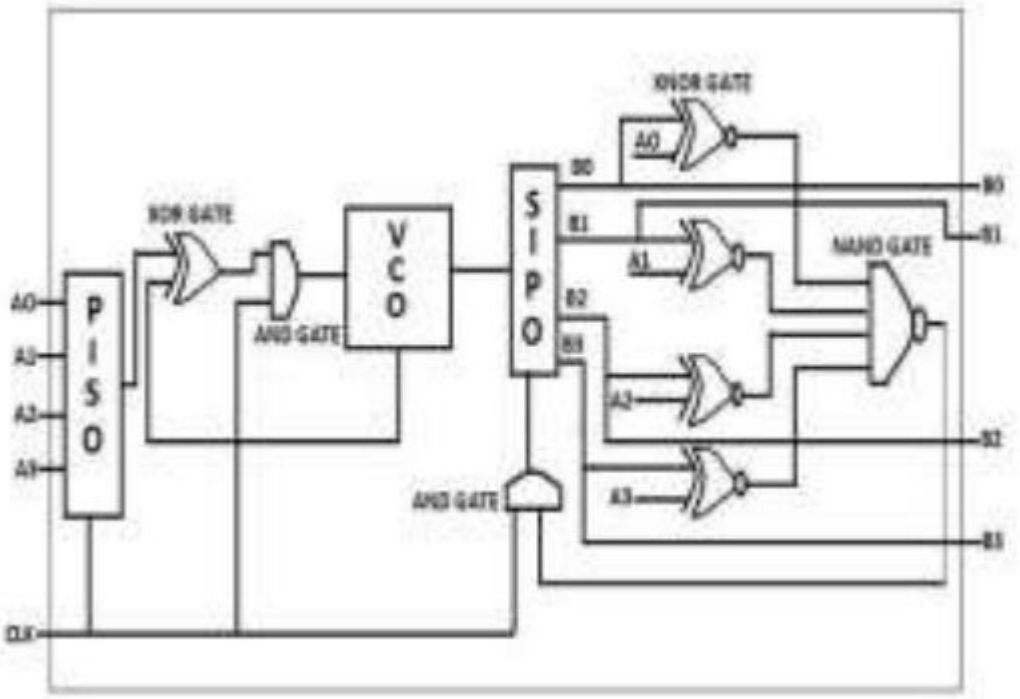

Figure 6: Counter based DPLL

- The PISO shift register is the first block in the diagram. It is designed so the 1st bit is fed to DPLL at clock one. The next bit is faded in the same way as mentioned.
- The second block is the phase detector used for detecting the phase existing between the reference and input signals. It is designed using XOR gate.
- The third block is the V_{CO}. It is designed using counter-based logic and the aim of V_{CO} is to produce the same bit as that of the input bit.
- The fourth block is the SIPO shift register.

EXPECTED OUTPUT WAVEFORM: -

Figure 7: Output waveform of Counter based DPLL

CONCLUSION: -In this conclusion we can conclude that there is a lot of pros and cons present here. The design choice is based on the type of application to be used and the most important parameter it is implemented .In most of the cases there is a trade between speed and design complexity of the circuit. MUX based DPLL is the most efficient approach when the speed is high and message signal bits can be sent parallelly. But this increases the complexity of the mux based DPLL which is overcome by the equivalent counter based DPLL system which corrects only one bit at a time.

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